

What is Claimed Is:

1. A method of manufacturing a semiconductor device having a PMOS transistor and an NMOS transistor, the method comprising:
  - forming a substrate comprising a layer of silicon (Si) having a strained lattice on a layer of silicon-germanium (SiGe);
  - forming isolation regions defining a PMOS region and an NMOS region;
  - forming a thermal oxide layer on the strained Si layer in the PMOS and NMOS regions;
  - selectively removing the thermal oxide layer and strained Si layer from the SiGe layer in the PMOS region;
  - depositing a layer of dielectric material on the layer of SiGe in the PMOS region; and
  - forming transistors in the PMOS and NMOS regions, wherein:
    - a portion of the thermal oxide layer serves as the gate dielectric layer of the NMOS transistor; and
    - a portion of the deposited layer of dielectric material serves as the gate dielectric layer of the PMOS transistor.
2. The method according to claim 1, comprising depositing a layer of material having a high dielectric constant (k) of 10 or higher as the layer of dielectric material on the layer of SiGe in the PMOS region.
3. The method according to claim 2, comprising depositing a material selected from the group consisting of silicon nitrides, silicon oxinitrides, metal oxides, metal silicates, metal aluminates, metal titanates, metal zirconates, ferroelectric materials, binary metal oxides and ternary metal oxides as the high dielectric constant (k) material.
4. The method according to claim 2, comprising:
  - forming the thermal oxide layer at a first thickness; and
  - depositing the layer of high dielectric constant (k) material at a second thickness greater than the first thickness.

5. The method according to claim 2, comprising depositing the layer of high dielectric constant (k) material at a thickness of 10 Å to 50 Å.

6. The method according to claim 5, comprising forming the thermal oxide layer at a thickness of 10 Å to 20 Å.

7. The method according to claim 2, comprising forming the thermal oxide layer at a thickness of 10 Å to 20 Å.

8. The method according to claim 4, comprising:  
forming the thermal oxide layer at a thickness of 10 Å to 20 Å; and  
depositing the layer of high dielectric constant (k) material at a thickness of 10 Å to 50 Å.

9. The method according to claim 2, comprising depositing the layer of high dielectric constant (k) material by chemical vapor deposition.

10. The method according to claim 2, comprising forming the transistors by:  
depositing a gate electrode layer;  
patterning to form a gate electrode in the PMOS region with the portion of the high dielectric constant (k) material thereunder as the gate dielectric layer, and to form a gate electrode in the NMOS region with a portion of the thermal oxide layer thereunder as the gate dielectric layer; and  
forming shallow source/drain extensions and deep source/drain regions.

11. The method according to claim 10, comprising sequentially:  
forming the shallow source/drain extensions;  
forming dielectric sidewall spacers on side surfaces of the gate electrode; and  
forming the deep source/drain regions.

12. A semiconductor device comprising:  
a substrate comprising a layer of silicon-germanium (SiGe);  
a PMOS transistor comprising:

a gate dielectric layer of a material having a high dielectric constant (k) of 10 or higher deposited on the layer of SiGe; and  
a gate electrode on the gate dielectric layer; and  
an NMOS transistor comprising:  
a layer of silicon (Si) having a strained lattice on the layer of SiGe;  
a thermally formed gate oxide layer on the layer of strained Si; and  
a gate electrode on the thermally formed gate oxide layer.

13. The semiconductor device according to claim 12, wherein the high dielectric constant (k) material is selected from the group consisting of silicon nitrides, silicon oxinitrides, metal oxides, metal silicates, metal aluminates, metal titanates, metal zirconates, ferroelectric materials, binary metal oxides and ternary metal oxides.

14. The semiconductor device according to claim 12, wherein the gate dielectric layer of the PMOS transistor has a thickness of 10Å to 50Å.

15. The semiconductor device according to claim 14, wherein the gate dielectric layer of the NMOS transistor has a thickness of 10Å to 20Å.

16. The semiconductor device according to claim 12, wherein the gate dielectric layer of the PMOS transistor has a thickness of 10Å to 50Å.

17. The semiconductor device according to claim 13, wherein the gate dielectric layer of the PMOS transistor is thicker than the gate dielectric layer of the NMOS transistor.

18. The semiconductor device according to claim 17, wherein :  
the gate dielectric layer of the PMOS transistor has a thickness of 10Å to 50Å; and  
the gate dielectric layer of the NMOS transistor has a thickness of 10Å to 20Å.